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Message from editor

Dear ECTI Association members

Thailand has passed the tough time in political issue, and now we are in the duration of reforming the country. Thai people expect the country will get back from the politic damages, and proceed as a democratic country soon.

In our academic field, many Thailand-loving foreign researchers have stopped to travel Thailand for a while, and now they come back so that the academic activities held in Bangkok and other places in Thailand will become boom again.

In this issue, I am proud to present you the artile entitled "Coding for Fault Tolerance in Disk Arrays" composed by Dr.Nattakan Puttarak, KMITL, paper list of ECTI-CIT Trans (Vol. 8, No. 1), reports from conference, and call-for-papers. As the president and committee of ECTI Association has been changed, and they just started the jobs, ECTI members may check their names in "ECTI Who's Who" in this issue.

ECTI E-Magazine Editor

Kosin Chamnongthai (KMUTT, Thailand)

In this issue:

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ECTI President Message:

This year we celebrate 12 years of the ECTI Association. The major conferences including ECTI-CON 2014 and ECTI-CARD 2014 organised by the ECTI were very successful in term of number of papers and quality. The ECTI magazine is another key activity of the ECTI Association this year. We have continuously published the ECTI magazine since 2007. The purpose of magazine is not only to provide knowledge related to all fields of electrical engineering but also to create a forum in order to bring together the members to discuss and exchange experiences. For the next decade, we will move forward to a high quality magazine very useful for all members.

As the president, I would like to express sincere appreciation to all the authors of this issue for their excellent contributions and editorial committee members for their great efforts to make this issue very successful. I also look forward to see the growing contribution for the magazine in the near future.

Prayoot Akkaraekthalin, KMUTNB

ECTI Transactions on Communication Engineering, Vol. 8, No. 2, April-June 2014

Coding for Fault Tolerance in Disk Arrays

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Abstract

A huge amount of data is required to be stored, updated, and transferred every day. Data storage is essential and necessary for data communications. Stand alone hard disk drive (HDD) is not enough to store such data, so disk arrays is one solution to efficiently apply with less expensive. However, disk arrays need reliable and efficient fault tolerance to recover disk failures which can occur from salient errors without any expectation/prediction. An MDS code, which is an optimal erasure code because it achieves the Singleton bound, is XOR-based erasure code that is suitable for disk arrays, but a good and flexible MDS code is not easy to be constructed. This article will review an EVENODD code that can correct 2 erasures, and introduce a new class of MDS code based on a graph structure, a CGR code, which can recover more than 3 erasures.

Keywords: MDS array codes, disk arrays, data storage, fault tolerance.

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Introduction

Nowadays, portable electronic equipments and gadgets become more popular because of their convenience and efficiency to use any time and everywhere. Not only the capacities of the battery to meet user needs, but also one of the most important aspect for portable devices is data storage such as hard disk drives (HDDs), flash drives, and others. Due to the increase of size of electronic files, if data storages get damages or work improperly, users might lose opportunity for business or precious information in their life.

For the sake of efficiency and worth the cost to store a huge amount of data in storage, disk array is one technique to efficiently store and transfer data. Disk array is managed by many HDDs working as a one storage system and allows data to be stored in a redundant, distributive, and balanced way to improve scalability, input/output throughput, and fault tolerance. This technique is easy to manage capacities and all sections in HDDs to store data, and also can protect some failures. The popular and well-known system based on this technique is Redundant Array of Independent Disk or RAID.

Generally, there are two techniques to protect and recover data from disk failures which are (1) replication disks, and (2) erasure-correction codes. The first method is easy to implement

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and not complexity, but wasted in resources. So, the second method is more worthwhile and efficient. However, a good erasure code with a capability to recover many disk failures is not easy to be constructed and implemented. A maximum distance separable (MDS) code is well-known in the most efficient erasure code because its characteristic to achieve the Singleton bound that one redundancy can protect and recover one disk failure. Moreover, an MDS code has less computational complexity than Reed-Solomon (RS) code using in RAID 6 since its encoding/ decoding process can be computed from a simple XOR operation and does not need to use a finite field.

An EVENODD code

Initially, an MDS code applied for disk arrays and known as the original of an MDS array code is an EVENODD code [1], which can protect and recover one failure disk. Fig. 1 shows an array structure of an EVENODD (7,5,2) code, when information disks and parity disks are separated in different columns.

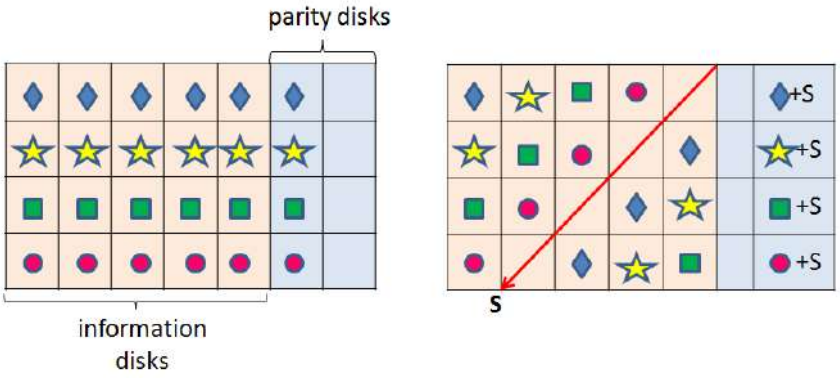

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Figure 1: A array structure of an EVENODD (7,5,2) code.

From Fig. 1 this code can protect disk arrays with 7 disks (equal to the number of columns) including 5 information disks and 2 parity disks (as known as redundancy). Therefore, it is presented as an EVENODD (7,5,2) code.

Definition: For any linear code (n,k,d) with a maximum distance; d = n-k+1, this code meets the Singleton bound and is an MDS code, where n is a number of total bits (or disks in disk arrays), and k is a number of information bits/ disks.

From Fig.1 and the definition of an MDS code, an EVENODD (7,5,2) code can recover damaged/ loss information stored in any 2 disks which is equal to a number of parity disks.

Moreover, an EVENODD code inspires more ideas and various techniques to construct an MDS array code that is able to protect and recover many failure disks, for example an X-codes [4] (can recover 2 disks as same as an EVENODD code, but it is a vertical array code that there are both information bits and parity bits contained in the same column (or disk)) yielded to a balance complexity in both encoding and decoding. Moreover, there are many types of erasure code applied for disk arrays which some is also an MDS code, but some is not such as a

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row-diagonal parity (RDP) array code [5], a STAR code (recover 3 disks and also be an MDS code) [6], and a HoVer code (recover more than 3 disks, but not an MDS code) [7].

Encoding and decoding process of an EVENODD code

A simple XOR operation is used in encoding/ decoding process of an EVENODD code where its complexity is computed in order to consider its performance as followings.

For an EVENODD code with an array of codeword is $(p-1)\times(p+2)$, where p is a prime number which is more than 0. So, a number of information bit columns (or a number of HDDs only stored information bits) is equal to p and a number of parity bit columns (or a number of HDDs only stored parity bits) is equal to 2.

At any symbol $a_{i,j}$ in a column of parity bits with row i^{th} and column j^{th},

Encoding process: $a_{i,p+1} = \sum_{t=1}^{p} a_{i,t}$ (1)

$$a_{i,p+2} = \sum_{t=1}^{p-1} a_{p-1-t,t} + S, \quad (2)$$

where $S = \sum_{t=1}^{p-1} a_{p-1-t,t} = \sum_{t=0}^{p-2} a_{i,p} + \sum_{t=0}^{p-2} a_{i,p+1}$ (3)

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Therefore, if $p = 5$, the EVENODD array code will be given as shown in Fig. 2.

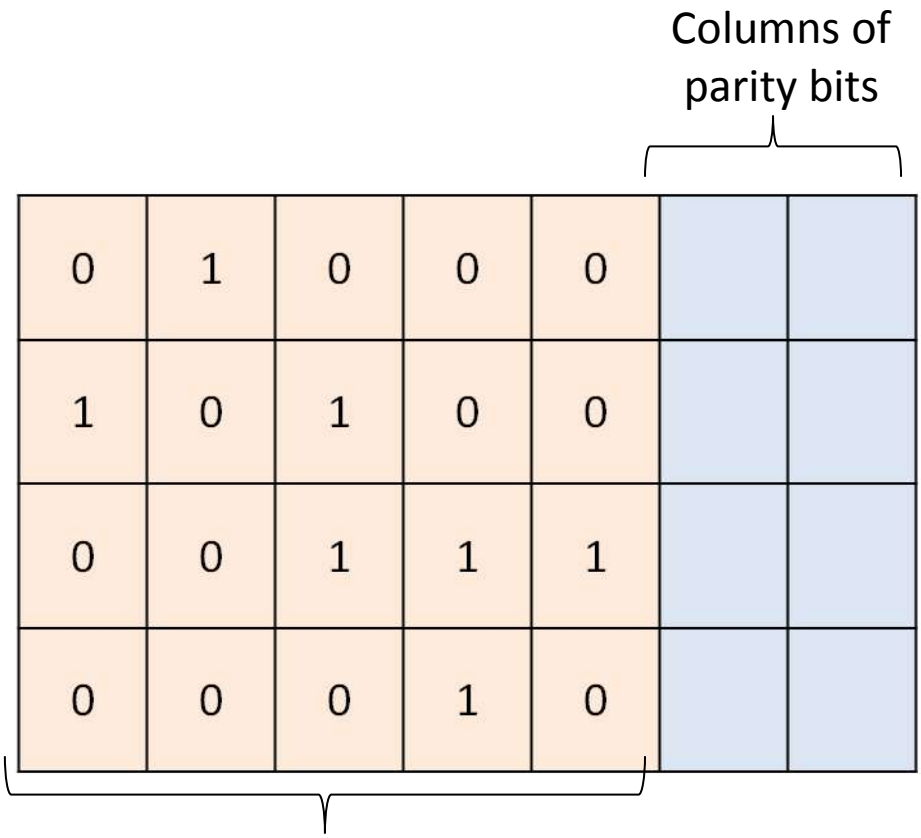

Figure 2: An array structure of an EVENODD code constructed from p=2.

From Fig. 2, all parity bits are computed by Eq. (1), (2), and (3), and stored in the last 2 columns. All parity bits for this example are shown in Fig. 3.

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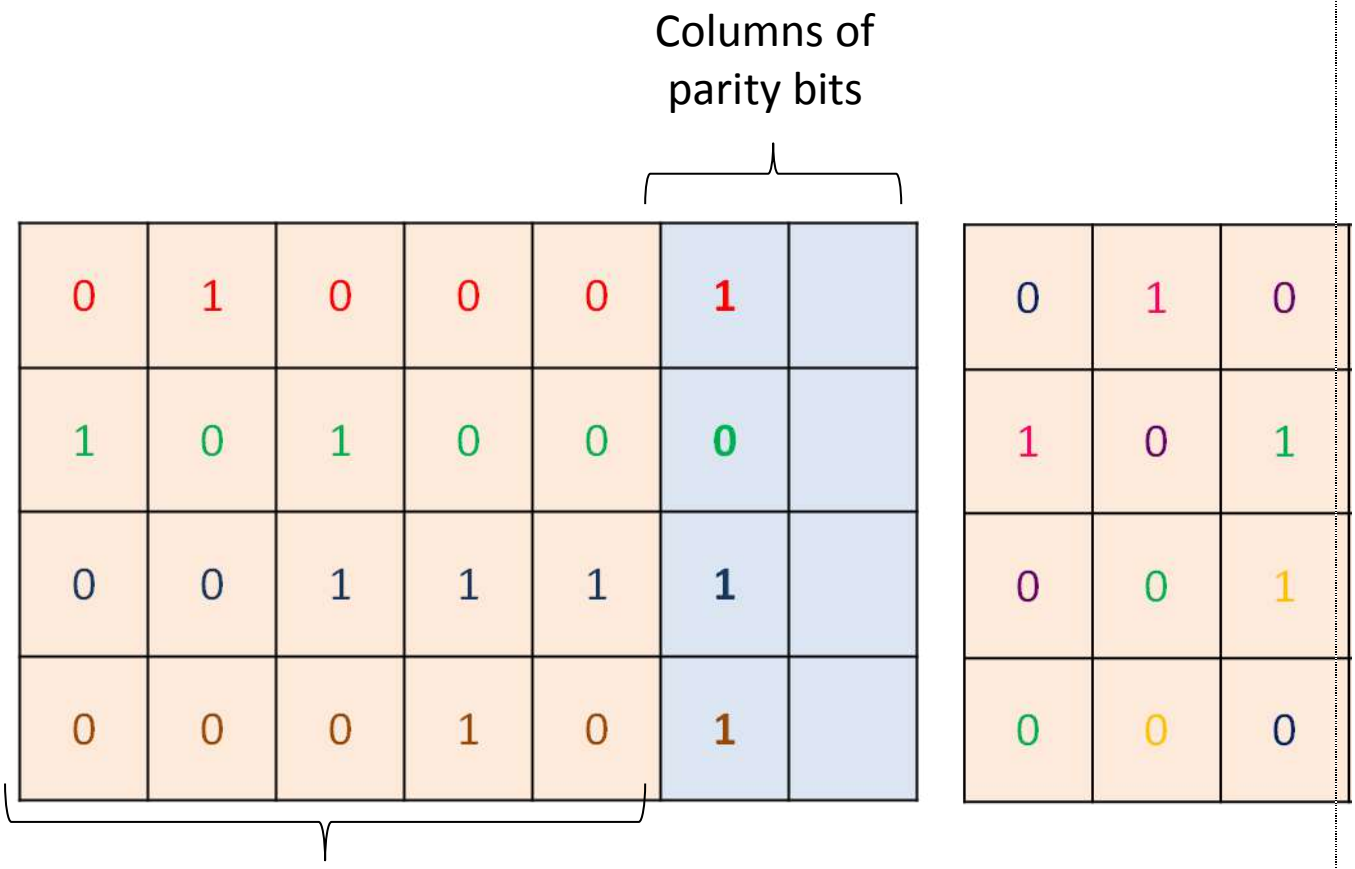

Figure 3: Parity bits in the first column (p1: left) and the second column (p2: right).

A codeword is in the form $[d_0 \quad d_1 \quad d_2 \quad d_3 \quad d_4 \quad | p_0 \quad p_1]$ in a code of disk arrays. So, in this EVENODD code, there are 4 codewords (since it has 4 rows in the array).

Typically, the loss of information stored in HDDs in disk arrays occurs when one or more HDDs are failed or get damaged. Assume that in this EVENODD (7,5,2) code, if there are 2 damaged disks in the same time, a decoding process will response to recover all loss bits by taking all survival symbols

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(all symbols that are not stored in those damaged disks) and XORing them until all loss data are completely recovered.

From an EVENODD (7,5,2) shown in Fig. 3, assume if two disks in an array which are represented by column 4 and 5 are damaged, all information bits stored in these two disks which are *a, b, c, d, e, f, g,* and *h* are also loss.

0	1	0	a	e	1	0
1	0	1	b	f	0	1
0	0	1	c	g	1	1
0	0	0	d	h	1	0

Figure 4: Assume that there are two damaged columns which are column 4 and 5.

The decoding process will be as following.

1. Compute a syndrome (S) from XORing all bits/ symbols from two columns of parity bits. So, $S = 1+0+1+1+0+1+1+0 = 1$.
2. Apply S for computing all loss data using XOR operation, where the concept of XOR operation is

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$$0+0=0$$
$$0+1=1$$
$$1+0=1$$
$$1+1=0$$

Thus, firstly, we can recover h from $h+0+0+0+S=h+0+0+0+1=1 => h=0$. Then, the remainders are computed by orders as followings.

$$0+0+0+d+h=0+0+0+d+0=1 \quad \Rightarrow d=1$$

$$d+g+1+1+S=1+g+1+1+1=1 \quad \Rightarrow g=1$$

$$0+0+1+c+g=0+0+1+c+1=1 \quad \Rightarrow c=1$$

$$0+c+f+0+S=0+1+f+0+1=0 \quad \Rightarrow f=0$$

$$0+0+1+a+S=0+0+1+a+1=0 \quad \Rightarrow a=0$$

$$0+1+0+a+e=0+1+0+0+e=1 \quad \Rightarrow e=0$$

$$0+1+b+e=0+1+b+0=S=1 \quad \Rightarrow b=0$$

3. Finally, the recovery is completed by XORing all survival bits from the related parity bits, and all recovered bits are shown in the array in Fig. 5.

0	1	0	0	0	1	0
1	0	1	0	0	0	1
0	0	1	1	1	1	1
0	0	0	1	0	1	0

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Figure 5: All data from decoding process.

To consider a complexity of both encoding and decoding process, we can compute from the number of XOR operations at the time that data get updated/ changed. For an EVENODD code, the encoding/ decoding complexity is computed from

$\frac{8\left(2p^2-2p-1\right)}{p-1}$ XOR operations.

In addition, an EVENODD code can correct errors and recover all loss/ damaged data when there are two failure disks at the same time (which is equal to a number of redundant disks.)

An MDS Array Code based on Graphs: a CGR code

Recently, there are many methods to design and construct an MDS array code for the sake of ability and flexibility in disk recovery and also protection in many disk failures. For example, a complete-graph-of-ring (CGR) code [3], [4] is constructed based on a graph structure called a complete graph of ring or CGR graph. The CGR code uses a CGR graph by referring their nodes as information bits and their edges as parity bits, then

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places all bits in the right position in an array, and takes a left-cyclic shift to assure that this code can be an MDS code. An example to construct the CRR (5,2) is shown as following procedures.

1) Construct a CGR graph.

To construct a CGR(5,2) code which has 5 bits (disks) and 2 information bits (disks), we need a CGR graph with 10 nodes and 15 edges. The CGR graph is constructed based on a complete graph, K_2 (which 2 nodes in this complete graph are called super nodes in a CGR graph). Then, we replace each super node with ring graph of 5 nodes, and replace the edge connecting 2 super nodes with 5 edges connecting 10 nodes from 2 rings together. So, there are totally 15 edges (10 edges from 2 rings plus 5 edges from the edge connecting 2 rings). This CGR graph is shown in Fig. 2.

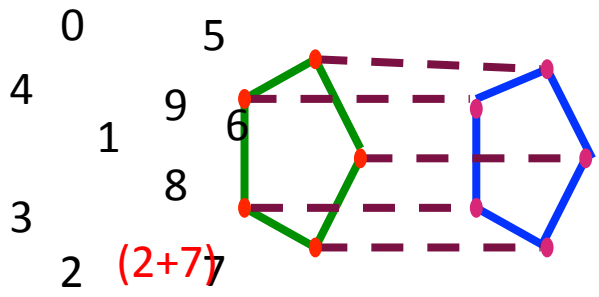

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Figure 2: The CGR graph for constructing the CGR (5,2) code.

2) Label all nodes and edges in a CGR graph.
From Fig. 2, we can label all nodes by numbers and all edges by XORing 2 numbers at both ends of the edge (in this figure, represented as symbol +) in order to place all nodes and edges in an appropriate position in an array. In this code, we clockwise label all nodes in each ring by order.

3) Place all nodes and edges into an array.
For the CGR code, the size of an array is related to a number of nodes and edges in a CGR graph [3], [4]. If a CGR (n,k) code is needed to be constructed based on n-nodes ring graph and (k+1)n edges, an array will consists of n columns and 2k+1 rows. Therefore, the array size for a CGR (5,2) code is 5x5. Then, place all nodes in each ring in a row one by one, so in this case the first and second rows store information bits, after that place all edges of each ring in the third and fourth rows, finally the last row belongs to 5 edges that connects 2 super nodes together. An array for a CGR (5,2) is shown in Fig. 3 (Left).

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However, this array code is not an MDS code yet. So, the last step is all rows in this array code needed to be left-cyclic shift by the offset 0, 1, 2, 2, 4 (the computation method is shown in 4]). This offset shows that the first row is not shifted, the second is shifted once so the first bit will be at the last column, the third and fourth bits are shifted twice so all bits in the first column will be at the fourth column, and the last row is shifted for four times so the first bit will be at the second column. The CGR (5,2) code which is also an MDS code is shown in Fig. 3 (Right).

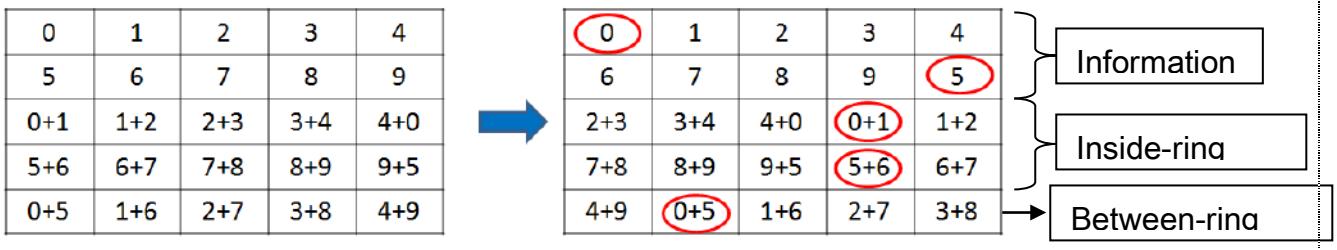

Figure 3: An array of a CGR (5,2) code.
Left: A CGR (5,2) code, Right: A CGR (5,2) code which is an MDS code.

A CGR code is capable of correcting up to 3, 5, 7, 9,… erasures depending on the structure of a CGR graph and its array size. From a CGR (5,2) code, there are 2 information disks, 3 parity disks, with a capability to recover up to 3 disks. Thus, this code is also an MDS code.

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Therefore, the properties of constructing a CGR code observed by the previous example are as followings. Let the number of information rows be $\frac{k}{d+2}$, which equals to the number of super nodes, where d is degree of all nodes, and k is a number of nodes.

a) The number of super node is equal to the number of rings.

b) The super graph is a symmetric graph and also can be a complete graph.

c) The information rows will be shifted by {0,1,2, …, the number of information rows -1}.

d) The inside-ring parity will be shifted by the same index, which equals to the number of rows.

e) The between-ring edges are shifted by 1. $\frac{k}{2(d+2)}$ edges are shifted by $\frac{k}{d+2}+2$. The edges $\left\{\left(\left[\frac{k}{d+2}-1\right],0\right),(1,2),(3,4),\ldots\right\}$ are in this set, and 2. The remaining edges can be grouped into $\frac{k}{d+2}$ sets, such that each set has $\frac{k}{2(d+2)}-1$ edges. Each set is shifted by $\left\{0,1,2,\ldots,\left(\frac{k}{d+2}-1\right)\right\}$.

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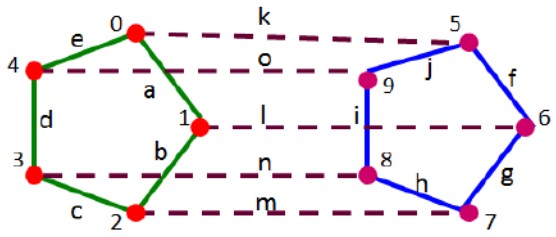
Moreover, the dual code of a CGR code is an MDS code, where the construction is also based on a CGR graph. Instead of using nodes to represent information bits, we use them to represent parity bits, and vice versa. For instance, from a CGR (5,2) code, the dual code will be constructed and its array is shown in Fig. 4.



a+e+k	a+b+l	b+c+m	c+d+n	d+e+o
f+g+l	g+h+m	h+i+n	i+j+o	j+f+k
c	d	e	a	b
h	i	j	f	g
o	k	l	m	n

Figure 4: A dual code of CGR (5,2) code.
Left: All labels for all nodes and edges. Right: Its dual CGR (5,2) code.

From Fig.4, we label all edges as shown in the left. Since all nodes represent parity bits, now all nodes are computed by XORing their attached edges. For example, node 0 is computed from $a+e+k$. Thus, to place all nodes and edges in an array, they are all at the same position as its original codes as shown in Fig. 4 (right). The first two rows are parity bits related to each information bit in the original code, while the information bits of the rest three rows come from each edge of a graph and also related to the parity bits of original code. Clearly, this dual code

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is also an MDS code, since its distance is 2, and it can recover up to 2 disk failures.

Conclusion

Fault tolerance in data storages is necessary and essential for reliable information/ data, which is stored and transferred every day. To protect and recover failure disks in disk arrays, an erasure code, especially an MDS code, is applied instead of adding replicated disks which are expensive. An EVENODD code is an MDS code using the simple XOR operation to compute parity bits. This code adds 2 parity disks, so it can protect and correct 2 erasures. After that there are many techniques to construct an MDS array code in order to improve their efficiency in terms of the number of erasures that they can recover, or a complexity reduction. A CGR code is another type of an MDS code which is constructed based on a graph called a CGR graph. This code is flexible to design and can correct more than 3 erasures depending on a CGR graph structure and a requirement of a CGR code. Also, its dual code is an MDS code and can correct 2 erasures.

References

วารสารอิเล็กทรอนิกส์ ECTI
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[1] M. Blaum, J. Brady, J. Bruck, and J. Menon, ``EVENODD: An Efficient Scheme for Tolerating Double Disk Failures in RAID Architectures", IEEE Trans. on Computers, vol.44, pp.192-202, Feb. 1995.

[2] A. G. Dimakis, K. Ramchandran, Y. Wu, and C. Suh, " A survey on Network Codes for Distributed Storages," Proceedings of the IEEE, vol.99, no.3, March 2011, pp. 476-489.

[3] P. Kaewprapha, N. Puttarak, and Jing Li (Tiffany), *"Nested Erasure Code to Achieve Singleton Bounds"*, Proceedings of the Conference on Information Sciences and Systems, CISS 2009.

[4] N. Puttarak, P. Kaewprapha, and Jing Li (Tiffany), *"A New Class of MDS Erasure Codes based on Graphs"*, Proceedings of the Global Telecommunications Conference, IEEE GLOBECOM, 2009.

[5] P. Corbett, B. English, A. Goel, T. Grcanac, S. Kleiman, J. Leong, and S. Sankar, *"Row-Diagonal Parity for Double Disk Failure Correction,"* Proceedings of the Third USENIX Conference on File and Storage Technologies, San Francisco, CA, USA, March 31–April 2, 2004.

[6] Z. Wang, A. G. Dimakis, and J. Bruck, *"Rebuilding for Array Codes in Distributed Storage Systems,"* CoRR, abs/1009.3291, 2010.

วารสารอิเล็กทรอนิกส์ ECTI
ECTI e-magazine
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[7] J. L. Hafner, *"HoVer Erasure Codes for Disk Arrays,"* IBM Research Report, Almaden Research Center, July 2005.

Nattakan Puttarak received her Ph.D in Electrical Engineering, Lehigh University (USA), in 2011, for her work in coding for data storage. She is currently a lecturer at the Telecommunications Engineering department, faculty of Engineering, King Mongkut's Institute of Technology Ladkrabang (KMITL), Thailand. Her research interests fall in coding theory in the area of data storage, including both the mainstream systems of hard drives and the emerging technology of flash drives. This includes designing new error correction coding strategies and decoding algorithms to combat disk failure and recover lost data for small-scale disk arrays as well as large-scale data centers, analyzing their performances, and identifying best practices.

Paper List of ECTI-CIT Trans., Vol. 8, No. 1, May-2014 issue

http://www.ecti-thailand.org/paper/journal/ECTI-CIT

Regular papers:

1. Abbas Mehdizadeh, Fazirulhisyam Hashim, Raja S. A. R. Abdullah, "Secure Group Communication Scheme in Wireless IPv6 Networks"
2. Thipwan Fangsuwannarak, "Thin Film preparation of silicon nano crystals embedded in silicon oxide by solgel method"
3. Jie Hu, Kou Yamada, Tatsuya Sakanushi, "The parameterization of all disturbance observers for time-delay plants with any input and output disturbances"
4. Yun Zhao, Kou Yamada, Tatsuya Sakanushi, Satoshi Tohnai, "A design method for robust stabilizing modified repetitive controllers for multiple-input/multiple-output time-delay plants with specified input-output characteristic"
5. Tanairat Mata, Katsuhiro Naito, Pisit Boonsrimuang, Hideo Kobayashi, "Proposal of Channel Estimation Method for ITS systems by using STBC MIMO-OFDM"

Special issue on Knowledge and Smart Technology:

6. Aji Prasetya Wibawa, "Augmented Javanese Speech Levels Machine Translation"
7. Wayan Firdaus Mahmudy, Romeo M Marian, Lee H S Luong, "Hybrid Genetic Algorithms for Part Type Selection and Loading Problem with Alternative Production Plans in Flexible Manufacturing System"
8. Vivek Kumar Singh, Rajesh Piryani, Ashraf Uddin, Pranav Waila, "Computing Sentiment Orientation of Textual Reviews at Document and Aspect Levels"
9. Songkran Kran Kantawong, "Exterior Climbing Mirror Cleaning Robot based on Hybrid Fuzzy-PID and Pneumatic Control System"
10. Supattra Puttinaovarat, Paramate Horkaew, Kanit Khaimook, "Assessing Deluge Predictability and Deterministic Attributes of Artificial Learning Systems"

Reported by Kosin Chamnongthai, associate editor of ECTI-CIT Trans

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Report from Conferences and Workshops

ECTI-CARD 2014, Chiang Mai, Thailand

6th Conference on Application Research and Development, ECTI-CARD for Peaceful World

ECTI-CARD 2014, the 6th annual conference organized by Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology Association of Thailand (ECTI Thailand) was held in Chiangmai Grandview Hotel, Changpuek, Muang, Chiangmai, Thailand, from May 21-23, 2014. The conference aims to promote application, research and development on all aspects of Computer Systems and Control including Artificial Intelligence, Computer Networks, DSP and Image Processing, Information Technology, Computing Theory, Bioinformatics, Knowledge Discovery, Information Retrieval, Grid and High performance

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computing, Natural Language Processing, Knowledge Management, Embedded System and Robotics, Software Engineering, Multimedia Analysis, Computer Visions and Graphics and E-commerce. The conference proceedings are published and accessible via ECTI website, http://www.ecti-thailand.org/.

The technical program included 3 keynote speeches, 1 workshop session, together with 1 dialogue session and 6 lecture sessions. Six best awards were announced in the conference banquet.

The Best Paper Award in 21PHY I Track

"Fabrication of Microparts using X-ray Lithography with Synchrotron Radiation"

R. Phatthanakun, S. Promwokorn, C. Sriphung, W. Pummara and N. Chomnawang

The Best Paper Award in 22ET Track

"An Original Verified System of the Video for CCTV"

Teerasak Kroputaponchai and Nikom Suvonvorn

The Best Paper Award in 21ArG I Track

"Development Infrared Rays Electric Oven with Closed Loop System"

Numchai Houysai, Pooyaphath

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Phumiphak and Saliltip Sintusontichart

The Best Paper Award in Dialogue P02 Track

"Development of FES for Foot-Drop Correction "DearnDee" in Thailand"

Jirawat Jitprasutwit, Ratikorn Chaiwattantham and Zeng Lerdmanorath

The Best Paper Award in Dialogue P04 Track

"Train Tracking and Position Error Correction Using Smart Phones"

Anan Charoenrat, Idrid Kaewdam, Sarawoot Rungraengwajiake and Pornchai Supnithi

The Best Paper Award in Dialogue P05 Track

"Single Phase Line Frequency Converter Didactic"

Surasak Yousawat, Suparak Srita and Uthen Kamnarn

Statistics & Facts about ECTI-CARD 2014

- There are 230 papers submitted
  and 152 papers accepted as regular papers.
- There are 19 invited papers submitted
- There are totally 171 papers from 41 universities.

Activities in ECTI-CARD 2014

ECTI-CARD 2014 prepared a series of social program, including a conference banquet with wonderful musical numbers as well as the Thai *Lanna traditional dance* for all registrants. There were also buffet banquet. **Chiang Mai** has its own very distinctive **culture**, arts, festivals, and traditions as well as an exciting mix of local, ethnic as well as expatriate communities from all over the world.

The next **ECTI-CARD 2015** will be held in Thumrin Thana Hotel, Trang, Thailand, from May 27-29, 2015. For more information, please go to the website http://ecticard2015.ecticard.org/.

วารสารอิเล็กทรอนิกส์ ECTI
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ECTI-CON 2014 is the 11th annual international conference organized by Electrical Engineering/ Electronics, Computer, Telecommunications and Information Technology (ECTI) Association, Thailand. The conference aims to be an international forum for presentation of technological advances and research results in the field of electrical engineering, electronics, computer, telecommunications, and information technology. Hosted by Suranaree University of Technology, during 14-17 May, 2014, the conference was held at the vibrant city of Nakhon Ratchasima, with its awesome historical sites and spectacular natural scenery that the north eastern of Thailand has to offer.

The conference was a success with 231 accepted papers from a total of 356 submissions, achieving an acceptance rate of 65%. The conference was attended by over 350 delegates from 17 countries.

Technical Program

The 231 accepted papers belong to 8 regular areas including,

- Device, Circuits and Systems
- Computers
- Information Technology
- Communication Systems
- Controls
- Electrical Power Systems
- Power Electronics
- Signal Processing

4 special sessions on

- Control applications
- Advanced Techniques in Applications, Signal Processing and Hardware Design
- Future Internet and New Network Services
- MIMO and Smart Antenna Technologies

Statistical submission data

Canada	1	Sri Lanka	8
China	10	Swaziland	1
Egypt	3	Sweden	1
India	26	Switzerland	1
Iran	12	Taiwan	4
Japan	16	Tanzania	3
Korea	2	Thailand	271
Kuwait	1	Turkey	3
Malaysia	8	United Kingdom	1
Myanmar	10	United States	2
Pakistan	7	Vietnam	7

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Keynotes speakers

Prof. Wg. Cdr. Dr. Sarawut Sujitjorn
Director of Synchrotron Light Research Institute (Publ. Org.), Thailand

Topic : Paralleled Induction Motors Drive: Modeling, Stability and Application.

Prof.Dr.Seiichi Shin
President of the Society of Instrument and Control Engineers, Japan.

Topic : A Future of Cars Driven by Electronics.

Prof.Dr. Apirat Siritaratiwat
KKU –Seagate Cooperation Research Laboratory, Khon Kaen University, Thailand.

Topic : Hard Disk Drive and the Future.

Student travel grants

ECTI-CON has achieved continued success over the past 11 years. Apart from upholding its reputation as an international forum for scientists and researchers, this year, for the very first time, ECTI-CON has offered student travel grants as an outreach to student delegates. A total of 15 student recipients from 7 countries namely, Sri Lanka, Vietnam, Japan, Malaysia, Egypt, India and Thailand have been carefully selected for the grant.

Best paper awards

This year out of 231 accepted papers, 5 papers have been carefully selected for best paper awards.

1. Power Electronics Area

"A Novel Three - Phase Three - Level ZVZCS DC-DC Converter Using Phase-Shift PWM Strategy"

By K. Thammachat and J. Anuwat from King Mongkut's Institute of Technology Ladkrabang, Thailand

2. Information Technology Area

"Development of a Trustworthy Authentication System in Mobile Ad Hoc

3. Control Area

"Criterion of Approximation for Designing 2 × 2 Feedback Systems with Inputs Satisfying Bounding Conditions"

By C. Tadchanon and A. Suchin from Chulalongkorn University, Thailand

4. Signal Processing Area

"Unsupervised Segmentation of Synthetic Aperture Radar Inundation Imagery Using the Level Set Method"

By P. Ponlapak and K. Teerasit from Kasetsart University, C. Thitiporn from NECTEC, R. Preesan from GISTDA, Thailand, K. Itsuo from Tokyo Institute of Technology, Japan

5. Communications Area

"A Short-term Rain-induced Attenuation Modelfor Satellite Link Quality Prediction"

By P. Jirutchaya,L. Tulaya, and P. N
Institute of Technology Ladkrabang,


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2015 – 7th International Conference on Knowledge and Smart Technology (*KST*)

January 28-31, 2015. Faculty of Informatics, Burapha University, Chon Buri, THAILAND.

"Entertainment Technology for Life"

Call for papers

KST international conference has been established with the aim in mind that a sustainable community will be achieved through continuous studies and share resources. The conference will be held annually in Burapha University which located in the Eastern part of Thailand. It provides a central forum for experts and developers to promote, share, and discuss various issues and developments in the broad field of Computational Intelligence, Intelligent Application, Intelligent Computer Networks and Systems, and Emerging Intelligent Technologies. KST international conference will provide an opportunity for young researchers to demonstrate their talent and interesting research ideas. The conference will benefit people who are actively involved in research related to computational intelligence and its applications. Accepted papers will be published in the KST-2015 Conference Proceedings. Presented and selected papers will be included in IEEEXplore®. Selected papers will be proposed for further extension before publishing in ECTI-Transaction on Computer and Information Technology (ECTI-CIT).

The list of topics of interest includes (but not limited to)

Computational Intelligence
- Artificial Immune Systems
- Bayesian Networks
- Cognitive Systems
- Computational neuroscience
- Data Analysis and Pattern Recognition
- DNA Computing
- Expert Systems
- Fuzzy Techniques and Systems
- Genetic Algorithms and Evolutionary Computing
- Knowledge-Based Systems (Knowledge Acquisition, Knowledge Discovery and Data Mining, Knowledge Representation and Management)
- Machine Learning
- Microarray Data Analysis
- Neural Networks
- Ubiquitous Computing

Intelligent Applications
- Bioinformatics using Intelligent & Machine Learning Techniques
- Fault Diagnosis
- Financial & Stock Market Monitoring and Prediction
- Geographical Information System
- Image & Signal and Time Series Processing
- Intelligent Disaster Warning System
- Intelligent Web-based Systems
- Machine & Computer Vision
- Medical & Diagnostic Systems
- Natural Language Processing
- Speech Processing and Synthesis

Intelligent Computer Networks and Systems
- Ad Hoc Networks
- Cloud and Grid Computing
- Computer Architecture
- Computer Simulation and Modeling
- Computer and Network Security
- Computer and Network Applications
- Computer Network and Communication
- Embedded Systems
- Network Management and Analysis
- Network Protocol and Architecture
- Mobile Computing and Systems
- Future Internet
- Parallel and Distributed Computing
- Pervasive and Mobile Computing
- Wireless Sensor Networks
- Wireless Networks and Communications

Emerging Intelligent Technologies
- Artificial Intelligence and Information Agents on the Internet
- Artificial Life
- Blind Source Separation
- Business Intelligence Systems
- Cognitive Interfaces
- Context-aware and Affective (Emotional) Computing
- Human-centered Computing
- Intelligent Operating Systems
- Intelligent Agents and Multi-Agent Systems
- Intelligent Tutoring Systems
- Intelligent User Interfaces
- Intelligent Web Mining & Applications
- Intelligent Web Personalization
- Semantic Web
- Multi- Media Intelligent Information Systems

Important Dates

Call for Special Session Proposal	July 15, 2014
Notification of Special Session	September 1, 2014
Full paper submission	October 1, 2014
Notification of acceptance	November 30, 2014
Registration	December 15, 2014
Camera-ready submission	December 15, 2014

Paper Submission

Full paper submission in English is expected. All manuscripts must be prepared in the standard IEEE Conference Proceedings format and limited to the maximum of 6 pages of A4 form in PDF format. Please use 10 points and Time New Roman font. The authors' names and affiliations, postal addresses, telephones, fax numbers and e-mail addresses must be omitted from the submitted manuscripts. Each manuscript must contain an abstract of about 100 words.

Conference site is **http://www.kst-thailand.org/**
Online submission site is **http://www.edas.info/N18217**

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ECTI-CON 2015

Hua Hin, Thailand June 24 – 26, 2015

ECTI-CON 2015 is the twelfth annual international conference organized by Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology (ECTI) Association, Thailand. The conference aims to provide an international platform to present technological advances, launch new ideas and showcase research work in the field of electrical engineering, electronics, computer, telecommunications and information technology. Accepted papers will be published in the Proceedings of ECTI-CON 2015 and will be submitted for inclusion into IEEE Xplore. Acceptance will be based on quality, relevance and originality.

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Area 1) Device, Circuits and Systems:
Semiconductor Devices, Analog Circuits, Digital Circuits, Mixed Signal Circuits, Nonlinear Nonlinear Circuits and Systems, Sensing and Sensor Networks, Filters and Data Conversion Conversion Circuits, RF and Wireless Circuits, Photonic and Optoelectronic Circuits, Low Low Power Design and VLSI Physical Design, Biomedical Circuits, Assembly and Packaging Packaging Technologies, Test and Reliability, Advanced Technologies (i.e. MEMS and Nano-Nano-electronic Devices, Metamaterials), Agritronics, Embedded Systems;

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Area 6) Electrical Power Systems:
Power Engineering and Power Systems, Electromagnetic Compatibility, Energy Conversion, Conversion, High Voltage Engineering and Insulation, Power Delivery, Power Electronics, Electronics, Illumination, Renewable/Alternative Energy, Energy Policy and Planning;

Area 7) Power Electronics:
Power Devices and Components, Power Quality Control, Harmonic Analysis and Compensations, Switching Circuits and Power Converters, Motor and Drives, Smart Grid, Grid, Distribution Generation and Electrical Vehicles, Photovoltaic Materials and Solar Cells; Cells;

Area 8) Signal Processing:
Signal Processing Theory, Digital Signal Processing Algorithms, Digital Filter Design & Implementation, Array Processing, Adaptive Signal Processing, Audio, Speech, and Language Processing, Image and Video Processing, Medical Signal Processing & Medical Imaging;

Special sessions:
The aim of special sessions is to provide researchers with an opportunity to present their their latest, cutting-edge research within specific fields relevant to the theme of the conference. Prospective organizers should submit proposals to the General Secretary via

Paper submission:

- Prospective authors are invited to submit original full papers **without author's names and affiliations, in English**, of 4-6 pages in standard IEEE two-column format only, reporting their original work and results, applications, and/or implementation in one or more of the listed topics.
- Papers must be submitted only by internet through the submission system of the conference website.
- At least one author of each accepted paper **MUST** register and present paper at the conference in order for the paper to be included in the program. The program will be submitted for inclusion into IEEE Xplore.

Important dates:

- Full paper submission: Jan 31, 2015
- Notification of acceptance: Apr 30, 2015
- Camera-ready paper submission: May 15, 2015
- Authors and Early-bird registration: May 15, 2015

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ECTI Association

IEEE THAILAND SECTION

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Asia-Pacific Signal and Information Processing Association Annual Summit and Conference 2014

December 9-12, 2014, Siem Reap, city of Angkor Wat, Cambodia
http://www.apsipa2014.org/

APSIPA ASC 2014

Call for Papers

Welcome to the APSIPA Annual Summit and Conference 2014 located in Siem Reap, city of Angkor Wat, the capital city in northwestern of Cambodia, and a popular resort town as the gateway to Angkor temples region. Siem Reap has colonial and Chinese-style architecture in the Old French Quarter. In the city, there are museums, traditional Apsara dance performances, silk farms, fishing villages and a bird sanctuary near the Tonle Sap Lake. The sixth annual conference is organized by Asia-Pacific Signal and Information Processing Association (APSIPA) aiming to promote research and education on signal processing, information technology and communications. The annual conference was previously held in Japan (2009), Singapore (2010), China (2011), USA (2012) and Taiwan (2013). The field of interest of APSIPA concerns all aspects of signals and information including processing, recognition, classification, communications, networking, computing, system design, security, implementation, and technology with applications to scientific, engineering, and social areas.

The regular technical program tracks and topics of interest include (but not limited to):

1 Biomedical Signal Processing and Systems (BioSiPS)
- 1.1 Biomedical Imaging
- 1.2 Modeling and Processing of Physiological Signals (EEG, MEG, EKG, EMG, etc.)
- 1.3 Biologically-inspired Signal Processing
- 1.4 Medical Informatics and Healthcare Systems
- 1.5 Genomic and Proteomic Signal Processing

2 Signal Processing Systems: Design and Implementation (SPS)
- 2.1 Nanoelectronics and Gigascale Systems
- 2.2 VLSI Systems and Applications
- 2.3 Embedded Systems
- 2.4 Video Processing and Coding
- 2.5 Signal Processing Systems for Data Communication

3 Image, Video, and Multimedia (IVM)
- 3.1 Image/video Coding
- 3.2 3D image/video Processing
- 3.3 Image/video Segmentation and Recognition
- 3.4 Multimedia Indexing, Search and Retrieval
- 3.5 Image/video Forensics, Security and Human Biometrics
- 3.6 Graphics and Animation
- 3.7 Multimedia Systems and Applications

4 Speech, Language, and Audio (SLA)
- 4.1 Speech Processing: Analysis, Coding, Synthesis, Recognition and Understanding
- 4.2 Natural Language Processing: Translation, Information Retrieval, Dialogue
- 4.3 Audio Processing: Coding, Source Separation, Echo Cancellation, Noise Suppression
- 4.4 Music Processing

5 Signal and Information Processing Theory and Methods (SIPTM)
- 5.1 Signal Representation, Transforms and Fast Algorithms
- 5.2 Time Frequency and Time Scale Signal Analysis
- 5.3 Digital Filters and Filter Banks
- 5.4 DSP Architecture
- 5.5 Statistical Signal Processing
- 5.6 Adaptive Systems and Active Noise Control
- 5.7 Sparse Signal Processing
- 5.8 Signal Processing for Communications
- 5.9 Signal Processing for Energy Systems
- 5.10 Signal Processing for Emerging Applications

6 Wireless Communications and Networking (WCN)
- 6.1 Wireless Communications: Physical Layer
- 6.2 Wireless Communications and Networking: Ad-hoc and Sensor Networks, MAC, Wireless Routing and Cross-layer Design
- 6.3 Wireless Networking: Access Network and Core Network
- 6.4 Security and Cryptography
- 6.5 Devices and Hardware

Submission of Papers

Prospective authors are invited to submit either full papers, up to 10 pages in length, or short papers up to 4 pages in length, where full papers will be for the single-track oral presentation and short papers will be mostly for poster presentation. Conference content will be submitted for inclusion into IEEE *Xplore* as well as other Abstracting and Indexing (A&I) databases.

Important Dates

Submission of Proposals for Special Sessions, Forum, Panel & Tutorial Sessions	~~May 9, 2014~~	June 6, 2014
Submission of Full and Short Papers	~~June 6, 2014~~	July 4, 2014
Submission of Papers in Special Sessions	July 4, 2014	
Notification of Papers Acceptance	Aug. 29, 2014	
Submission of Camera Ready Papers	Sep. 26, 2014	
Author Registration Deadline	Sep. 26, 2014	
Tutorial Session Date	Dec. 9, 2014	
Summit and Conference Dates	Dec. 9-12, 2014	

E-mail : secretary@apsipa2014.org

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